What is claimed is:

1. A method of forming an electronic device, the method comprising:

forming a first electrode;

forming a dielectric oxide layer on the first electrode wherein the dielectric oxide layer includes titanium, wherein a first portion of the dielectric oxide layer adjacent the first electrode has a first density of titanium, and wherein a second portion of the dielectric oxide layer opposite the first electrode has a second density of titanium different than the first density; and

forming a second electrode on the dielectric oxide layer so that the dielectric oxide layer is between the first and second electrodes.

2. A method according to Claim 1 wherein the dielectric oxide layer further includes tantalum.

3. A method according to Claim 1 wherein the dielectric oxide layer comprises tantalum titanium oxide.

4. A method according to Claim 1 wherein forming the first electrode comprises forming the first electrode on a substrate so that the first electrode is between the substrate and the dielectric oxide layer.

5. A method according to Claim 1 wherein the first density of titanium is greater than the second density of titanium.

6. A method according to Claim 5 wherein the first density of titanium is in the range of approximately 0.1 to 15 percent.

7. A method according to Claim 5 wherein the second density of titanium is in the range of approximately 0.001 to 3 percent.

8. A method according to Claim 1 wherein the first density of titanium is less than the second density of titanium.

9. A method according to Claim 8 wherein the first density of titanium is in the range of approximately 0.1 to 15 percent.

10. A method according to Claim 8 wherein the second density of titanium is in the range of approximately 10 to 20 percent.

11. A method according to Claim 1 wherein each of the first and second electrodes comprises at least one of doped polysilicon, metal, metal oxide, metal nitride, and/or metal oxynitride.

12. A method according to Claim 1 further comprising:

forming a reaction suppressing layer between the first electrode and the dielectric layer.

13. A method according to Claim 12 wherein the reaction suppressing layer comprises at least one of silicon nitride, silicon oxide, and/or silicon oxynitride.

14. A method of forming an electronic device, the method comprising:

forming a first electrode;

forming a reaction suppressing layer on the first electrode;

forming a dielectric oxide layer on the reaction suppressing layer so that the reaction suppressing layer is between the first electrode and the dielectric oxide layer and wherein the dielectric oxide layer includes titanium; and

forming a second electrode on the dielectric oxide layer so that the dielectric oxide layer is between the reaction suppressing layer and the second electrode.

15. A method according to Claim 14 wherein the reaction suppressing layer comprises at least one of silicon nitride, silicon oxide, and/or silicon oxynitride.

16. A method according to Claim 14 wherein the dielectric oxide layer further includes tantalum.

17. A method according to Claim 14 wherein the dielectric oxide layer comprises tantalum titanium oxide.

18. A method according to Claim 14 wherein forming the first electrode comprises forming the first electrode on a substrate so that the first electrode is between the substrate and the reaction suppressing layer.

19. A method according to Claim 14 wherein a first portion of the dielectric oxide layer adjacent the reaction suppressing layer has a first density of titanium, and wherein a second portion of the dielectric oxide layer opposite the reaction suppressing layer has a second density of titanium different than the first density.

20. A method according to Claim 19 wherein the first density of titanium is greater than the second density of titanium.

21. A method according to Claim 20 wherein the first density of titanium is in the range of approximately 0.1 to 15 percent.

22. A method according to Claim 20 wherein the second density of titanium is in the range of approximately 0.001 to 3 percent.

23. A method according to Claim 19 wherein the first density of titanium is less than the second density of titanium.

24. A method according to Claim 23 wherein the first density of titanium is in the range of approximately 0.1 to 15 percent.

25. A method according to Claim 23 wherein the second density of titanium is in the range of approximately 10 to 20 percent.

26. A method according to Claim 14 wherein each of the first and second electrodes comprises at least one of doped polysilicon, metal, metal oxide, metal nitride, and/or metal oxynitride.

27. An electronic device comprising:

a first electrode;

a dielectric oxide layer on the first electrode wherein the dielectric oxide layer includes titanium, wherein a first portion of the dielectric oxide layer adjacent the first electrode has a first density of titanium, and wherein a second portion of the dielectric oxide layer opposite the first electrode has a second density of titanium different than the first density; and

a second electrode on the dielectric oxide layer so that the dielectric oxide layer is between the first and second electrodes.

28. An electronic device according to Claim 27 wherein the dielectric oxide layer further includes tantalum.

29. An electronic device according to Claim 27 wherein the dielectric oxide layer comprises tantalum titanium oxide.

30. An electronic device according to Claim 27 further comprising a substrate on the first electrode so that the first electrode is between the substrate and the dielectric oxide layer

31. An electronic device according to Claim 27 wherein the first density of titanium is greater than the second density of titanium.

32. An electronic device according to Claim 31 wherein the first density of titanium is in the range of approximately 0.1 to 15 percent.

33. An electronic device according to Claim 31 wherein the second density of titanium is in the range of approximately 0.001 to 3 percent.

34. An electronic device according to Claim 27 wherein the first density of titanium is less than the second density of titanium.

35. An electronic device according to Claim 34 wherein the first density of titanium is in the range of approximately 0.1 to 15 percent.

36. An electronic device according to Claim 34 wherein the second density

of titanium is in the range of approximately 10 to 20 percent.

37. An electronic device according to Claim 27 wherein each of the first and second electrodes comprises at least one of doped polysilicon, metal, metal oxide, metal nitride, and/or metal oxynitride.

38. An electronic device according to Claim 27 further comprising a reaction suppressing layer between the first electrode and the dielectric layer.

39. An electronic device according to Claim 38 wherein the reaction suppressing layer comprises at least one of silicon nitride, silicon oxide, and/or silicon oxynitride.

40. An electronic device comprising:

a first electrode;

a reaction suppressing layer on the first electrode;

a dielectric oxide layer on the reaction suppressing layer so that the reaction suppressing layer is between the first electrode and the dielectric oxide layer and wherein the dielectric oxide layer includes titanium; and

a second electrode on the dielectric oxide layer so that the dielectric oxide layer is between the reaction suppressing layer and the second electrode.

41. An electronic device according to Claim 40 wherein the reaction suppressing layer comprises at least one of silicon nitride, silicon oxide, and/or silicon oxynitride.

42. An electronic device according to Claim 40 wherein the dielectric oxide layer further includes tantalum.

43. An electronic device according to Claim 40 wherein the dielectric oxide layer comprises tantalum titanium oxide.

44. An electronic device according to Claim 40 further comprising a substrate on the first electrode so that the first electrode is between the substrate and

the reaction suppressing layer.

45. An electronic device according to Claim 40 wherein a first portion of the dielectric oxide layer adjacent the reaction suppressing layer has a first density of titanium, and wherein a second portion of the dielectric oxide layer opposite the reaction suppressing layer has a second density of titanium different than the first density.

46. An electronic device according to Claim 45 wherein the first density of titanium is greater than the second density of titanium.

47. An electronic device according to Claim 46 wherein the first density of titanium is in the range of approximately 0.1 to 15 percent.

48. An electronic device according to Claim 46 wherein the second density of titanium is in the range of approximately 0.001 to 3 percent.

49. An electronic device according to Claim 45 wherein the first density of titanium is less than the second density of titanium.

50. An electronic device according to Claim 49 wherein the first density of titanium is in the range of approximately 0.1 to 15 percent.

51. An electronic device according to Claim 49 wherein the second density of titanium is in the range of approximately 10 to 20 percent.

52. An electronic device according to Claim 40 wherein each of the first and second electrodes comprises at least one of doped polysilicon, metal, metal oxide, metal nitride, and/or metal oxynitride.

53. A semiconductor memory device comprising:

a semiconductor substrate;

a lower electrode formed on the semiconductor substrate;

a dielectric layer which is an oxide film including titanium and tantalum, on an

upper surface of the lower electrode; and

an upper electrode on an upper surface of the dielectric layer,

wherein the density of titanium in the dielectric layer depends on the thickness of the dielectric layer.

54. The semiconductor memory device of claim 53, wherein the density of titanium of an area of the dielectric layer adjacent to the lower electrode is 0.1 to 15 percent.

55. The semiconductor memory device of claim 53, wherein a reaction suppressing layer is further interposed between the lower electrode and the dielectric layer so as to prevent a reaction between the lower electrode and the dielectric layer.

56. The semiconductor memory device of claim 55, wherein the reaction suppressing layer is one of a silicon nitride film, a silicon oxide film, and a silicon oxynitride film.

57. The semiconductor memory device of claim 53, wherein the lower electrode and the upper electrode are formed of at least one conductive film selected from a doped polysilicon film, a metal film, a metal oxide film, a metal nitride film, and a metal oxynitride.

58. A semiconductor memory device comprising:

a semiconductor substrate;

a lower electrode formed on the semiconductor substrate;

a reaction suppressing layer formed on an upper surface of the lower electrode;

a first tantalum titanium oxide film formed on an upper surface of the reaction suppressing layer;

a second tantalum titanium oxide film formed on an upper surface of the first tantalum titanium oxide film; and

an upper electrode formed on an upper surface of the second tantalum titanium oxide film,

wherein the density of titanium of the first tantalum titanium oxide film is 0.1 to 15 percent and the density of titanium of the second tantalum titanium oxide film is higher than or equal to the density of titanium of the first tantalum titanium oxide film.

59. The semiconductor memory device of claim 58, wherein the density of titanium of the second tantalum titanium oxide film is 0.001 to 3 percent.

60. The semiconductor memory device of claim 58, wherein the density of titanium of the second tantalum titanium oxide film is 10 to 20 percent.

61. The semiconductor memory device of claim 58, wherein the reaction suppressing layer is one of a silicon nitride film, a silicon oxide film, and a silicon oxynitride film.

62. The semiconductor memory device of claim 58, wherein the lower electrode and the upper electrode are formed of at least one conductive film selected from a doped polysilicon film, a metal film, a metal oxide film, a metal nitride film, and a metal oxynitride.

63. A method for manufacturing a semiconductor memory device, the method comprising:

(a) forming a lower electrode on an upper surface of a semiconductor substrate;

(b) forming a dielectric layer of a oxide film including titanium and tantalum, on an upper surface of the lower electrode; and

(c) forming an upper electrode on an upper surface of the dielectric layer,

wherein, in step (b), the density of titanium in the dielectric layer depends on the thickness of the dielectric layer.

64. The method of claim 63, wherein, in step (b), the density of titanium is adjusted to be 0.1 to 15 percent.

65. The method of claim 63, wherein the method further comprises forming a reaction suppressing layer for suppressing a reaction between the lower electrode and the dielectric layer, between steps (a) and (b).

66. The method of claim 65, wherein the reaction suppressing layer is one of a silicon nitride film, a silicon oxide film, and a silicon oxynitride film.

67. The method of claim 66, wherein the reaction suppressing layer is formed by applying one of a rapid thermal nitridation, a rapid thermal oxidation, and a combination thereof to a surface of the lower electrode.

68. The method of claim 66, wherein the reaction suppressing layer is formed by chemical vapor deposition.

69. The method of claim 63, wherein step (b) further comprises:

separately supplying a titanium precursor, a tantalum precursor, and oxygen gas into a reactor; and

reacting the titanium precursor, the tantalum precursor, and the oxygen gas with each other within the reactor.

70. The method of claim 69, wherein the tantalum precursor is one of a metal alkoxide such as $Ta(OC_2H_5)_5$, an organometalic such as a metal beta deketonate, and a metal halide such as $TaCl_5$.

71. The method of claim 69, wherein the titanium precursor is a compound such as one of $Ti(OCH(CH_3)_2)_4$, $Ti(OC_2H_5)_4$, $TiCl_4$, and a tetrakis-dimethylamido-titanium (TDMAT).

72. The method of claim 63, wherein, in step (b), the tantalum precursor and the titanium precursor are mixed outside of the reactor and the mixed substance is supplied into the reactor.

73. The method of claim 72, wherein the tantalum precursor is pentaethoxy tantalum $Ta(OCH_2CH_3)_6$, (PET) and the titanium precursor is tetraethoxy titanium $Ti(OCH_2CH_3)_4$, (TET).

74. The method of claim 72, wherein a density of titanium in the dielectric layer is controlled by the deposition temperature and the flow rate of the precursor.

75. The method of claim 72, wherein the dielectric layer is formed under a temperature of 100 to 700°C and a pressure of 100 to 760mTorr.

76. The method of claim 75, wherein the tantalum precursor and the titanium precursor are provided at a rate of 5 to 200mg/min and the oxygen gas is supplied at a rate of 10sccm to 10slm.

77. The method of claim 63, wherein the method further comprises applying a thermal process to the dielectric layer under an oxygen atmosphere, between steps (b) and (c).

78. A method for manufacturing a semiconductor memory device, the method comprising:

(a) forming a lower electrode on an upper surface of the semiconductor substrate;

(b) forming a reaction suppressing layer on an upper surface of the lower electrode;

(c) forming a first tantalum titanium oxide film on an upper surface of the reaction suppressing layer;

(d) forming a second titanium oxide film on an upper surface of the first tantalum titanium oxide film;

(e) applying a thermal process to the first and the second tantalum titanium oxide films under an oxygen atmosphere; and

(f) forming an upper electrode on an upper surface of the second tantalum titanium oxide film,

wherein a density of titanium is adjusted to be 0.1 to 15 percent when the first tantalum titanium oxide film is formed and a density of titanium of the second tantalum titanium oxide film is higher than or equal to the density of titanium of the first tantalum titanium oxide film.

79. The method of claim 78, wherein a density of titanium of the second tantalum titanium oxide film is 0.001 to 3 percent.

80. The method of claim 78, wherein a density of titanium of the second tantalum titanium oxide film is 10 to 20% percent.

81. The method of claim 78, wherein the reaction suppressing layer is one of a silicon nitride film, a silicon oxide film, and a silicon oxynitride film.

82. The method of claim 81, wherein the reaction suppressing layer is formed by applying one of a rapid thermal nitridation, a rapid thermal oxidation, or a combination thereof to a surface of the lower electrode.

83. The method of claim 81, wherein the reaction suppressing layer is formed by chemical vapor deposition.

84. The method of claim 78, wherein steps (c) and (d) further comprise:

separately supplying a titanium precursor, a tantalum precursor, and oxygen gas into a reactor; and

reacting the titanium precursor, the tantalum precursor, and the oxygen gas with each other within the reactor.

85. The method of claim 84, wherein the tantalum precursor is one of a metal alkoxide such as $Ta(OC_2H_5)_5$, an organometalic such as a metal beta deketonate, and a metal halide such as $TaCl_5$.

86. The method of claim 84, wherein the titanium precursor is a compound such as one of $Ti(OCH(CH_3)_2)_4$, $Ti(OC_2H_5)_4$, $TiCl_4$, and a tetrakis-dimethylamido-titanium (TDMAT).

87. The method of claim 78, wherein, in steps (c) and (d), the tantalum precursor and the titanium precursor are mixed outside of the reactor and the mixed substance is supplied into the reactor.

88. The method of claim 87, wherein the tantalum precursor is pentaethoxy tantalum $Ta(OCH_2CH_3)_6$, (PET) and the titanium precursor is tetraethoxy titanium $Ti(OCH_2CH_3)_4$, (TET).

89. The method of claim 87, wherein a density of titanium in the dielectric layer is controlled by the deposition temperature and the flow rate of the precursor.

90. The method of claim 87, wherein the tantalum titanium oxide film is formed under a temperature of 100 to 700°C and a pressure of 100 to 760mTorr.

91. The method of claim 90, wherein, in steps (c) and (d), the tantalum precursor and the titanium precursor are provided at a rate of 5 to 200mg/min and the oxygen gas is supplied at a rate of 10sccm to 10slm.

92.A dielectric layer for an electronic device, the dielectric layer comprising:

a dielectric oxide layer including titanium wherein a first portion of the dielectric oxide layer has a first density of titanium and wherein a second portion of the dielectric oxide layer has a second density of titanium different than the first density.

93.A dielectric layer according to Claim 92 wherein the dielectric oxide layer further includes tantalum.

94.A dielectric layer according to Claim 92 wherein the dielectric oxide layer comprises tantalum titanium oxide.

95.A method of forming a dielectric oxide layer for an electronic device, the method comprising:

forming a first portion of the dielectric oxide layer having a first density of titanium; and

forming a second portion of the dielectric oxide layer having a second density of titanium different than the first density.

96.A method according to Claim 95 wherein the dielectric oxide layer further includes tantalum.

97.A method according to Claim 95 wherein the dielectric oxide layer comprises tantalum titanium oxide.